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10/053,963	01/22/2002	Aron T. Lunde	MICS:0214	5214

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/053,963	LUNDE, ARON T.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28* is/are allowed.

6)☒ Claim(s) *1,2,5,8-10,13-15,18,19,21-23,26 and 27* is/are rejected.

7)☒ Claim(s) *3,4,6,7,11,12,16,17,20,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5, 8-10, 13-15, 18, 19, 21-23, 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shibata (U.S. Patent 5,661,407).

In re claim 1, **Shibata** discloses a method for forming a die, the method comprising, forming a die 1 on a wafer, the die 1 having one or more lateral edges, an active portion 1c comprising integrated circuitry, and an inactive portion formed between the active portion and at least one lateral edge of the one or more lateral edges of the die 1, wherein the die 1 has a plurality of input bond pads 2 formed on the active portion 1c (col. 6, lines 14-20 and FIG. 4);

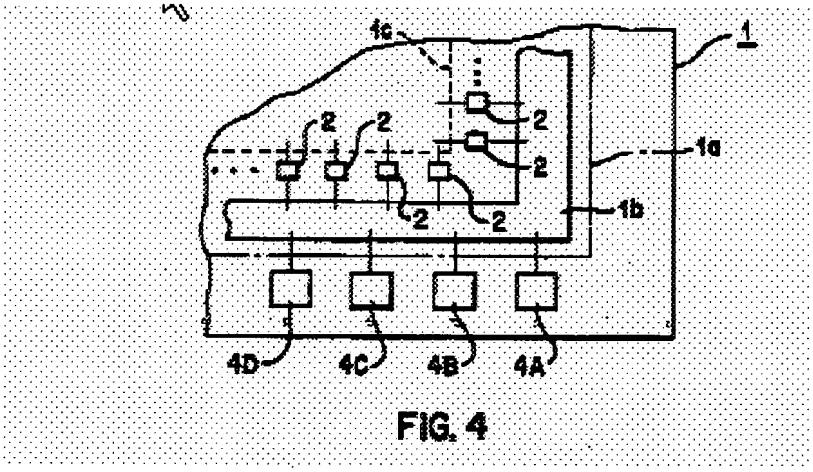

FIG. 4

forming at least one test pad 4A-D (col. 6, line 29) on the die 1; and forming a conductive path (wire bonding) (col. 6, lines 27-28) between the at least one input bond pad 2 and the at least one test pad 4A-D, wherein a portion of the conductive path is formed on the inactive portion of the die between the at least one lateral edge of the die 1 and the active portion 1c of the die 1 (col. 6, lines 26-35 and FIG. 4).

In re claim 2, as applied to claim 1 above, **Shibata** discloses all claimed limitations including the limitation wherein the plurality of test pads 4A-D is formed on the active portion 1c of the die 1 (col. 6, lines 13-21).

In re claim 5, as applied to claim 1 above, **Shibata** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside of the active portion of the die 1 (col. 6, lines 32-34).

In re claim 8, as applied to claim 1 above, **Shibata** discloses all claimed limitations including the limitation wherein at least one test pad 4A-D is of a sufficient size so as to be accessible by a testing apparatus (col. 4, lines 45-51).

In re claim 9, **Shibata** discloses a die assembly formed on a wafer, the die assembly comprising, a die 1 formed on a wafer, the die 1 having one or more lateral edges, an active portion 1c comprising integrated circuitry, and an inactive portion formed between the active portion 1c and at least one lateral edge of the one or more lateral edges of the die 1; at least one input bond pad 2 formed on the active portion of the die 1 (col. 6, lines 14-20 and FIG. 4);

at least one test pad 4A-D (col. 6, line 29) formed entirely on the die 1; and a conductive path (wire bonding) (col. 6, lines 27-28) that electrically couples the at least

one input bond pad 2 to the at least one test pad 4A-D, wherein a portion of the conductive path is formed on the inactive portion between the at least one lateral edge of the die 1 and the active portion of the die 1 (col. 6, lines 26-35 and FIG. 4).

In re claim 10, as applied to claim 9 above, **Shibata** discloses all claimed limitations including the limitation wherein the plurality of test pads 4A-D is formed on the active portion 1c of the die 1 (col. 6, lines 13-21).

In re claim 13, as applied to claim 9 above, **Shibata** discloses all claimed limitations including the limitation wherein at least one test pad 4A-D is of a sufficient size so as to be accessible by a testing apparatus (col. 4, lines 45-51).

In re claim 14, **Shibata** discloses a method for preparing a die on a wafer for testing by a testing apparatus, the method comprising, forming a die 1 on a wafer, the die 1 having one or more lateral edges, an active portion 1c comprising integrated circuitry, and an inactive portion formed between the active portion 1c and at least one lateral edge of the one or more lateral edges of the die 1; forming a plurality of input bond pads 2 on the active portion 1c (col. 6, lines 14-20 and FIG. 4);

forming a plurality of test pads 4A-D (col. 6, line 29) entirely on the die 1, wherein the plurality of test pads 4A-D accessible to the testing apparatus (col. 4, lines 45-51), at least one of the plurality of test pads 4A-D corresponding to at least one of the plurality of input bond pads 2; forming a conductive path (wire bonding) (col. 6, lines 27-28) between the at least one of the plurality of test pads 4A-D and the at least one of the plurality of input bond pads 2, wherein a portion of the conductive path is formed on the active portion between the at least one lateral edge of the die and the active portion 1c of

the die 1 (col. 6, lines 26-35 and FIG. 4); and testing the die 1 by contacting the at least one of plurality of test pads 4A-D with the testing apparatus (col. 8, lines 58-65).

In re claim 15, as applied to claim 14 above, **Shibata** discloses all claimed limitations including the limitation wherein the plurality of test pads 4A-D is formed on the active portion 1c of the die 1 (col. 6, lines 13-21).

In re claim 18, as applied to claim 14 above, **Shibata** discloses all claimed limitations including the limitation wherein severing the conductive path at a point outside of the active portion 1c of the die 1 (col. 6, lines 32-34).

In re claim 19, as applied to claim 16 above, **Shibata** discloses all claimed limitations including the limitation wherein severing the conductive path at a point within the inactive portion (FIG. 4).

In re claim 21, as applied to claim 14 above, **Shibata** discloses all claimed limitations including the limitation wherein at least one of the plurality of test pad 4A-D is larger in size than the at least one of the plurality of the input bond pads 2 (col. 6, lines 16-17 and FIG. 4).

In re claim 22, **Shibata** discloses a die comprising: one or more lateral edges; an active portion 1c comprising integrated circuitry; an inactive portion formed between the active portion 1c and at least one lateral edge of the one or more lateral edges of the die 1, a plurality of input bond pads 2 formed on the active portion 1c (col. 6, lines 14-20 and FIG. 4);

a plurality of test pads 4A-D (col. 6, line 29) formed entirely on the die 1, and the plurality of conductive lines (wire bonding) (col. 6, lines 27-28), wherein each of the

conductive lines is initially formed to electrically couple at least one of the plurality of input bond pads 2 to at least one of the plurality of test pads 4A-D, and wherein a portion of each of the conductive lines is formed on the inactive portion between the at least one lateral edge of the die 1 and the active portion 1c of the die 1 (col. 6, lines 26-35 and FIG. 4).

In re claim 23, as applied to claim 22 above, **Shibata** discloses all claimed limitations including the limitation wherein the plurality of test pads 4A-D is formed on the active portion 1c of the die 1 (col. 6, lines 13-21).

In re claim 26, as applied to claim 25 above, **Shibata** discloses all claimed limitations including the limitation wherein the portion of each of the conductive lines is configured to be severed when the die 1 is separated from the wafer (col. 6, lines 32-34).

In re claim 27, as applied to claim 22 above, **Shibata** discloses all claimed limitations including the limitation wherein the at least one of the plurality of test pads 4A-D is larger in size than the at least one of the plurality of input bond pads 1 (col. 6, lines 16-17).

Allowable Subject Matter

3. Claim 28 is allowed over prior art of record

4. Claims 3, 4, 6, 7, 11, 12, 16, 17, 20, 24 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons For Allowance

5. The following is an examiner's statement of reasons for allowance:

After further search and consideration of Applicant's response filed on May 07th, 2007 (see Applicant's response in Page 11 of the May 07th, response), it is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole taken alone or in combination, in particular, prior art of record does not teach "wherein a portion of said each of said conductive lines is formed on a scribe area outside the die", as recited in the independent claim 28.

Response to Applicant's Amendment and Arguments

6. Applicants' arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendment filed on May 07th, 2007.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER

/KN/
July 30, 2007